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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,235	10/24/2003	Young-Kyun Cho	SAM-0496	1427

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Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
TRA, ANH QUAN	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,235	CHO, YOUNG-KYUN	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9 and 11* is/are rejected.

7)☒ Claim(s) *4,8,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Ingino, Jr. (USP 6441660).

As to claims 1 and 9, Ingino, Jr. discloses in figure 3 a differential charge pump, and a method thereof, comprising: a first driver (M_y, M_{S2}) for receiving a first input signal (Down) and generating a first output signal (signal at node between the transistors); a second driver (the PMOS and NMOS transistors that receive signal Up in box 42) for receiving a second input signal (Up) and generating a second output signal (at node between the transistors); a third driver (M_{S1}, M_x) for receiving an inverted signal (/Up) of the second input signal and generating a third output signal (at node between the transistors) having the same voltage level as the first output signal; a fourth driver (the PMOS and NMOS transistor that receive signal /Down in box 40) for receiving an inverted signal (/Down) of the first input signal and generating a fourth output signal (at node between the transistor) having the same voltage level as the second output signal; a first transistor (M_{c2}) having a gate connected to a first bias voltage (voltage at the gate of transistor M_{m2}), a source to which the first output signal is applied, and a drain connected to an output signal (V_{Ctrl}) of a first differential charge pump; a second transistor (transistor, in box 42, which coupled to transistors M_{c2} and M_{m2}) having a gate connected to the first bias voltage, a

source to which the second output signal is applied, and a drain connected to an output signal (V_{Dummy}) of a second differential charge pump; a third transistor (M_{c1}) having a gate connected to the second bias voltage (at the gate of transistor M_{m3}), a source to which the third output signal is applied, and a drain connected to an output signal of the first differential charge pump: and a fourth transistor (transistor, in 40, which coupled to transistors M_{c1} and M_{m3}) having a gate connected to a second bias voltage, a source to which the fourth output signal is applied, and a drain connected to the output signal of the second differential charge pump.

As to claim 2, figure 3 shows that the first input signal is a down signal, and the second input signal is an up signal, and the first to the fourth drivers are buffers.

As to claim 3, figure 3 shows that the first input signal is an inverted down signal, and the second input signal is an inverted up signal, and the first to the fourth drivers are inverters.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross (USP 6466070) in view of Ingino, Jr. (USP 6441660).

Ross's figure 2 shows a phase locked loop having a phase detection means (110) for detecting a phase difference between a reference clock signal (x(t)) and a desired clock signal (y(t)) and generating a first input signal (DOWN), a second input signal (UP), an inverted signal of the first input signal (/DOWN) and an inverted signal of the second input signal (/UP); a

differential charge pump (120) for receiving the first input signal, the second input signal, the inverted signal of the first input signal and the inverted signal of the second input signal as input signals and generating an output signal (122) of a first differential charge pump and an output signal (124) of a second differential charge pump; a loop filter (126) for charging and discharging in response to the output signal of the first differential charge pump and the output signal of the second differential charge pump; and a voltage controlled oscillator (130, 140) for receiving the output signal of the first differential charge pump and the output signal of the second differential charge pump as input signals and controlling the phase of the desired clock signal. Thus, figure 2 shows all limitations of the claims except for the detail of the differntial charge pump circuit. However, Ingino, Jr.'s figure 3 shows a differential charge pump having all the claimed elements. Ingino, Jr.'s differential charge pump has no or substantially small error in a low supply voltage condition, thereby improving the circuit performance. Therefore, it would have been obvious to one having ordinary skill in the art to use Ingino, Jr.'s differential charge pump for Ross's differential charge pump for the purpose of improving the circuit performance in a low supply voltage condition.

Allowable Subject Matter

5. Claims 4, 8, 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4, 8, 10 and 12 would be allowable because the prior art fails to teach the differential charge pump, and a method thereof, further comprising: a common mode feedback circuit for receiving the output of the reference voltage, the output signal of the first differential

charge pump and the output signal of the second differential charge pump as inputs and generating the first bias voltage; and a fifth transistor having a drain and a gate connected to the second bias voltage, and a source connected to the ground voltage.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

October 15, 2004